REMARKS

Applicant respectfully requests reconsideration of this application in view of the foregoing amendments and the following remarks.

Claim Status

Claims 1-19 are pending in this application. Claims 1-19 have been rejected. Claims 10-19 are herein amended. No new matter has been added by these amendments.

Objections to the Specification

The Examiner has objected to the Abstract of the Disclosure because it has 218 words, which is over the 150 word limit prescribed by the MPEP § 608.01(b).

Applicant has amended the Abstract of the Disclosure to be within the word limit prescribed by the MPEP. Accordingly, Applicant respectfully submits that this objection is overcome or otherwise rendered moot and respectfully requests that it be withdrawn.

Rejection Under 35 U.S.C. § 112

Claims 10-19 have been rejected under 35 U.S.C. § 112, second paragraph, as containing a limitation lacking antecedent basis. Applicant has amended claims 10-19 to provide sufficient antecedent basis for the limitations therein. Accordingly, reconsideration and withdrawal of this rejection is respectfully requested.

Rejections Under 35 U.S.C. § 103(a)

Claims 1-19 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,448,725 (Gervais) in view of U.S. Patent No. 5,596,796 (Byers).

With respect to independent claims 1 and 9, the Examiner asserted that Gervais teaches, inter alia, an error detecting circuit comprising, "a data storing unit for dividing a circuit implemented in a chip into predetermined areas ... and outputting a plurality of

error signals in response to a plurality of error signals ... a lock enable signal ... and a chip error signal...", and "an error data collecting unit for outputting the chip error signal ... in response to the plurality of signals output from the error data storing unit". In addition, the Examiner asserted that Gervais "fails to teach a serial chain signal, the serial chain signal for reading the plurality of state error signals stored in the chip if the chip goes out of order when the error occurs in the circuit", and "in response to the serial chain signal, enables confirmation of at least one of the plurality of state error signals stored in the error data storing unit".

The Examiner further asserted, however, that Byers teaches "a serial scan chain composed of a plurality of scan latches, holding collected errors, is scanned out, confirming the state of the stored errors". Thus, according to the Examiner "one with ordinary skill in the art would find it obvious that a scan chain would require a scan enable signal in order to scan out a serial chain, even though the art did not specify such a signal". Applicant respectfully disagrees.

Claim 1 of the present invention recites,

> An error detecting circuit comprising:
> an error data storing unit for dividing a circuit implemented in a chip into predetermined areas, and outputting a plurality of error signals in response to a plurality of state error signals, a serial chain signal, a lock-enable signal, and a chip error signal, each of the plurality of state error signals being enabled when an error occurs in a corresponding predetermined area, the serial chain signal for reading the plurality of state error signals stored in the chip if the chip goes out of order when the error occurs in the circuit, and the lock-enable signal for determining whether or not to preserve the plurality of state error signals; and
> an error data collecting unit for outputting the chip error signal in response to the plurality of error signals output from the error data storing unit,

wherein the error data storing unit stores and outputs at least one of the plurality of state error signals and, in response to the serial chain signal, enables confirmation of at least one of the plurality of state error signals stored in the error data storing unit.

Byers, on the other hand, discloses a method and apparatus for identifying and indicating the severity of a fault within a computer system. In particular, Byers discloses a computer system having an error reporting scheme. The error reporting scheme consists of an error detection register and a group lock control block. A number of error detection units are provided in the system and each of the error detection units may assert an error bit within a corresponding error detection unit. Upon detection of an error, Byers generates an error bit at an error detection unit and provides it to an error detection register. A group lock control bit may then be provided to the error detection register from a group lock control block that freezes the state of an error detection register. The contents of the error detection register may then be scanned out by a support controller.

Byers, does not, however, disclose a serial chain signal for reading the plurality of state error signals stored in the chip if the chip goes out of order when the error occurs in the circuit. Instead, Byers discloses using the support controller to scan out the contents of the error detection registers after receiving an indication from the error detection registers. Byers does not disclose scanning out the contents of the error detection registers using a serial chain signal, rather Byers discloses scanning out the contents via an interface.

In addition, even if Byers were to use a serial chain signal to scan out the contents of its error detection registers, Byers, either alone or in combination with Gervais, still does not teach or suggest outputting the chip enable signal to the error detection unit

when an error is detected and, in response to the serial chain signal, enabling confirmation of at least one of the plurality of state error signals stored in the data storing unit as claimed by the present invention.

Accordingly, neither Byers nor Gervais, either alone or in combination, discloses or suggests at least "a serial chain signal for reading the plurality of state error signals stored in the chip if the chip goes out of order when the error occurs in the circuit...", and outputting a chip enable signal to "an error data collecting unit [that] stores and outputs at least one of the plurality of state error signals and, in response to the serial chain signal, enables confirmation of at least one of the plurality of state error signals stored in the error data storing unit" as recited in claim 1 of the present invention. As such, Applicant believes that the invention as recited in independent claims 1 and 9 is patentable over the cited art for at least the reasons stated.

Dependent Claims

Applicant has not independently addressed the rejections of the dependent claims because Applicant submits that, in view of the amendments to the claims presented herein and, for at least similar reasons as why the independent claims from which the dependent claims depend are believed allowable as discussed, *supra*, the dependent claims are also allowable. Applicant however, reserves the right to address any individual rejections of the dependent claims should such be necessary or appropriate.

CONCLUSION

Accordingly, Applicant submits that the claims as herein presented are allowable over the prior art of record, taken alone or in combination, and that the respective rejections be withdrawn. Applicant further submits that the application is hereby placed in condition for allowance which action is earnestly solicited.

Respectfully submitted,

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